**1.**

Question 1

What was missing in CPLDs that created a need for devices like FPGAs ?

**1 / 1 point**



Designs that required many flip-flops



Designs that contained large amounts of sequential circuits



All of the above

**Correct**

Completely correct.

**2.**

Question 2

Which of the following characterize CPLDs ? (**Select all that apply**)

**1 / 1 point**



LUTs



Scales easily to larger devices



Predictable

**Correct**

Correct. CPLDs have predictable timing because of the fixed routing structure



Rich with FFs/registers



Easy to design with

**Correct**

Correct. CPLDs have a clear structure and good software tools that make them easy to design with.



Deterministic

**Correct**

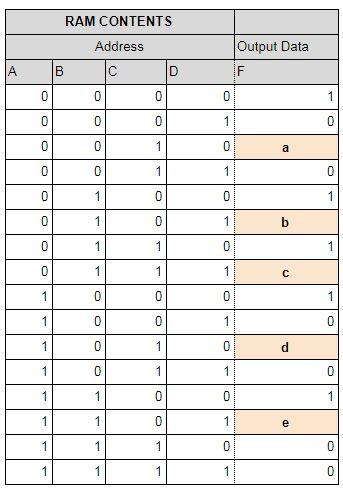
Correct. CPLDs have deterministic timing.

**3.**

Question 3

Fill in the table so that the LUT implements:

**F = (~A & B) | (~C & ~D)**



a = \_\_

b = \_\_

c = \_\_

d = \_\_

e = \_\_

Enter your numerical answers separated by a comma

(example:***x,x,x,x,x*** or **1,1,1,1,1**)

**1 / 1 point**

0,1,1,0,0

**Correct**

**4.**

Question 4

Which of the following characteristics best match a **CPLD** and which best match an **FPGA**?

**1 / 1 point**



***CPLD :***PLDs that are an integrated circuit designed to be configured by the designer after manufacturing and made up of memory elements (LUTs) and registers.

***FPGA :***A PLD with multiple PALs in the same package with registered outputs and an interconnecting programmable fabric.



***CPLD :***PLDs that are an integrated circuit designed to be configured by the designer after manufacturing and made up of memory elements (LUTs) and registers.

***FPGA :***A PLD with a fixed AND plane and a programmable OR plane.



***CPLD :***A PLD with multiple PALs in the same package with registered outputs and an interconnecting programmable fabric.

***FPGA :***PLDs that are an integrated circuit designed to be configured by the designer after manufacturing and made up of memory elements (LUTs) and registers.



***CPLD :***A PLD with a fixed AND plane and a programmable OR plane.

***FPGA :***PLDs that are an integrated circuit designed to be configured by the designer after manufacturing and made up of memory elements (LUTs) and registers.

**Correct**

Correct for both!

**5.**

Question 5

Which of the following set of characteristics best matches **LUTs**.

**0 / 1 point**



PLDs with a fixed OR plane and a programmable AND plane



PLDs with a fixed AND plane and a programmable OR plane



Memory elements that are the basic elements of the device



PLDs with multiple PALs in the same package with registered outputs and an interconnecting programmable fabric



Is a semiconductor device integrated circuit (IC) product that is dedicated to a specific application market and sold to more than one user



Is a semiconductor device integrated circuit (IC) product that is dedicated to a specific company



PLDs that are an integrated circuit designed to be configured by the designer after manufacturing and made up of memory elements (LUTs)

**Incorrect**

A Look-up table usually a portion of a device, not the entire device.

**6.**

Question 6

Which of the following is the best definition for a **CPLD ?**

**1 / 1 point**



A device with multiple PALs in same package with registered outputs and interconnecting programmable fabric



A device with a combination of fully re-programmable AND/OR array and a bank of macrocells that perform combinational and sequential logic



An array of programmable logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together", like many logic gates that can be inter-wired in different configurations

**Correct**

Correct, this is a good description of a CPLD.

**7.**

Question 7

Select 3 characteristics that are associated with **Antifuse FPGAs** ?

( **Select all that apply** )

**0.6666666666666666 / 1 point**



High Reliability

**Correct**

Correct, Antifuse FPGAs have high reliability relative to other types, and can be radiation hardened.



Highest Density



Reprogrammable



Expensive



One time Programmable (OTP)

**Correct**

Correct, Antifuse FPGAs can only be programmed once; after that the fuse pattern is set.



Lowest Cost

**This should not be selected**

SRAM FPGAs are lower cost than Antifuse for the same amount of logic and package size.

**8.**

Question 8

How many**4-input LUTs** with single outputs will be required to implement a **2-bit full adder**with carry?

**1 / 1 point**



2



4



1



3

**Correct**

Correct, 4 LUTs are required to make a 2-bit adder.

**9.**

Question 9

Does the usage of LUTS for implementation of adders with respect to gates improve delay or performance? Select all that apply..

**1 / 1 point**



decreases delay

**Correct**

True, as the number of gate delays will be larger than the number of LUT delays. The result of the implementation of the 4-bit ripple-carry adder in the Altera MAX10 FPGA is made of a cascade of 4 pairs of 3-input LUTs. The delay through this circuit will be only 4 LUT delays, not 11 gate delays as based on the delay equation of Carry Look ahead adder.



increases delay



increases performance

**Correct**

This is also correct



decreases performance

**10.**

Question 10

Which of the characteristics describe the implementation of a multiplier in an FPGA using Hard Multipliers versus implementation in Memories ? (**Mark all that apply**)

**1 / 1 point**



**Hard Multipliers**: Fast

**Correct**

Correct, Hard multipliers are optimized for speed.



**Hard Multipliers**: Slow



**Memories**: Do not scale easily , Lookup Tables

**Correct**

Correct. Multipliers built of memory do not scale easily as the memory size of the look- up table grows exponentially.



**Memories**: Complex , Lookup Tables

**11.**

Question 11

Which of the characteristics match the implementation of a multiplier in an FPGA using Speciality Circuits, such as the Booth Algorithm ? ( **Mark all that apply )**

**0.75 / 1 point**



Fast

**Correct**

Correct, Booth Algorithm multipliers are fairly fast in execution time



Big



Small

**Correct**

Correct. Booth algorithm multipliers are fairly small in area especially for larger multiplicands



Slow



Complex

**Correct**

Correct. Booth algorithm multipliers are more complex than shifter or memory types



Do not scale easily



Lookup Tables

**This should not be selected**

Booth algorithm multipliers use shift registers and adders, no lookup tables



State Machine

**12.**

Question 12

Which one of the following is **not** a programmable logic device?

**1 / 1 point**



EPROM



PLA



CPLD



ROM



FPGA

**Correct**

Correct. A ROM’s bit pattern is set during manufacturing of IC and can’t be changed.

**13.**

Question 13

What is true for ASICs relative to FPGAs? (Select all that may apply)

**1 / 1 point**



Lower speed



ASICs have lower cost per unit.

**Correct**

Correct. ASICs have lower cost per unit.



Higher speeds

**Correct**

Correct. ASICs generally have higher speed than FPGAs



High cost per unit

**14.**

Question 14

What are the principal advantages of FLASH based FPGAs over SRAM based FPGAs ? (**Mark all that apply**)

**1 / 1 point**



Faster Speed



Lower Power

**Correct**

Correct. FLASH FPGAs have lower leakage and consume much less static power.



Higher Reliability

**Correct**

Correct. FLASH FPGAs are more reliable, with SEU immunity



Better Security

**Correct**

Correct. FLASH FPGAs are a single chip solution that is difficult to reverse engineer once the security fuse is blown.

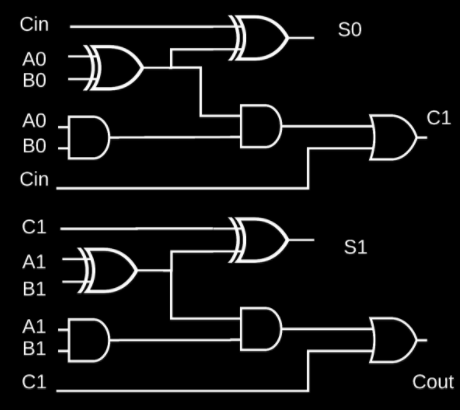
**15.**

Question 15

Which of the following is the best implementation for a 2-bit full adder. Hint: make sure to pay attention to signal names as well as circuit diagram.

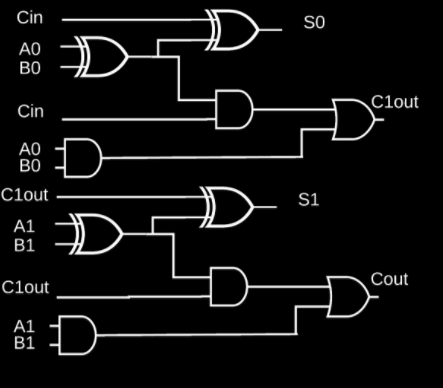
**0 / 1 point**





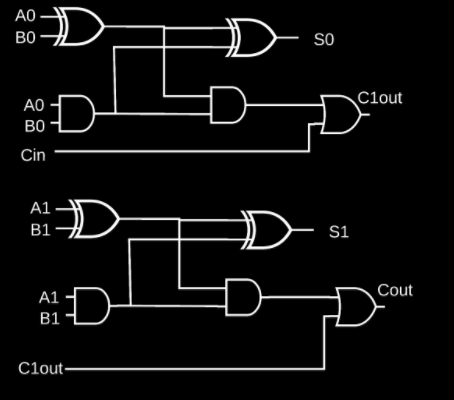
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**Incorrect**

If you missed this, you might want to review Video 6

**16.**

Question 16

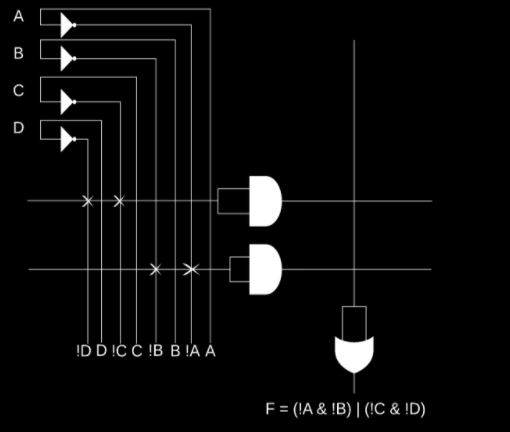
**Choose the best implementation of the logic equation**

**(NOT(A) AND NOT(B)) OR (NOT(C) AND NOT(D))**

**using PLA options:**

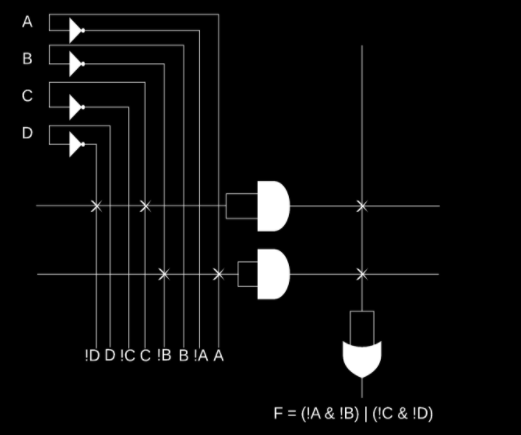
**0 / 1 point**





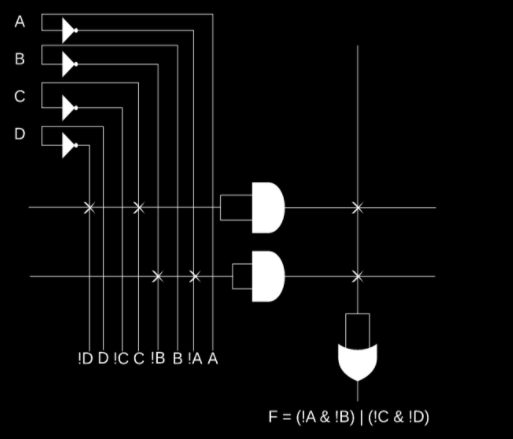
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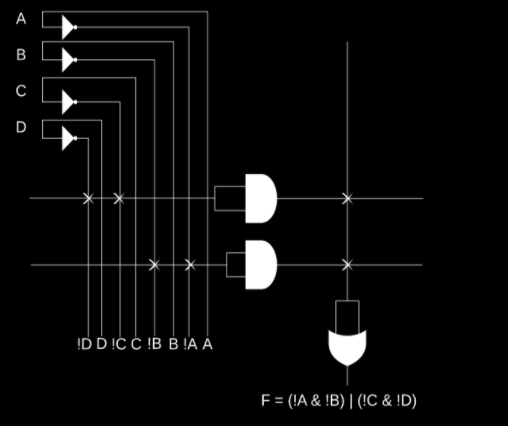
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**Incorrect**

If you missed this, you might want to review Video 5

**17.**

Question 17

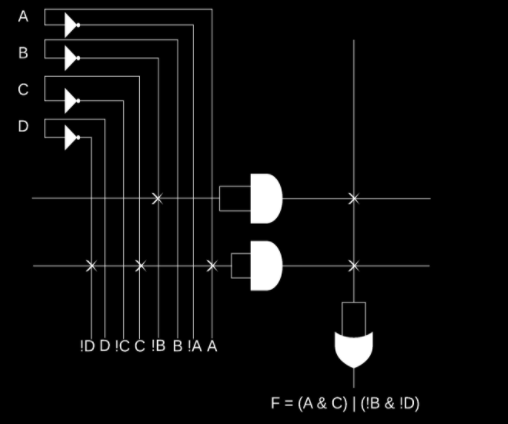
**Choose the correct implementation of logic equation**

**((A) AND (C)) OR (NOT(B) AND NOT(D))**

**using PLA options:**

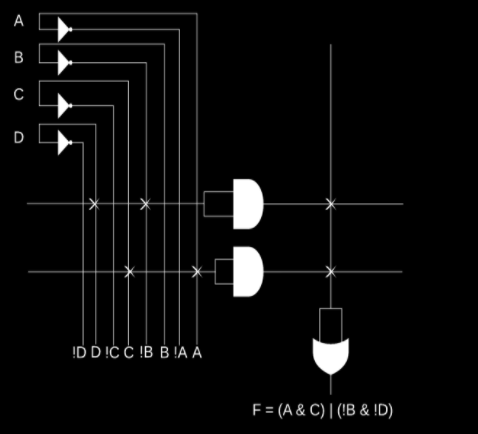
**1 / 1 point**





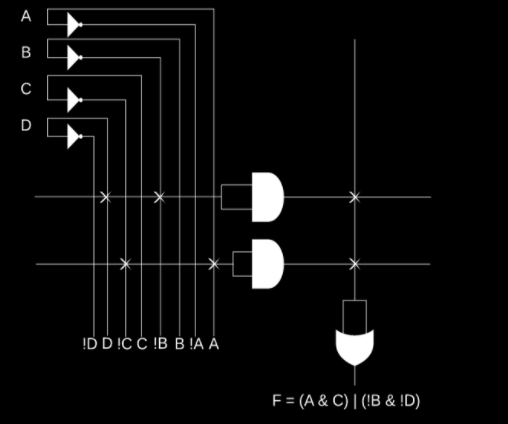
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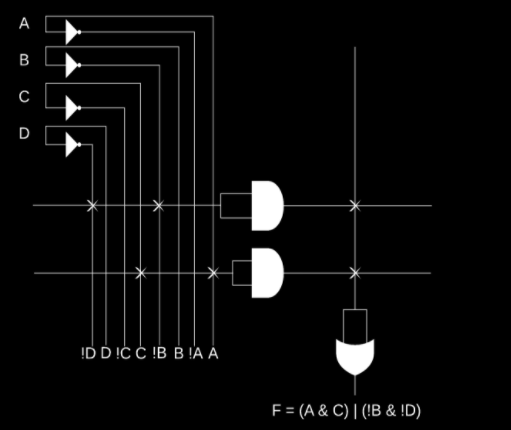
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**Correct**